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CPE 322

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**Simulation Assignment**

This document contains my submission for the simulation assignment, problems 1-6. They will be separated into 6 different sections with code and answers to the questions provided in the document.

**Section 1 – Ring Oscillator**

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| Non-blocking output (inv [8:0])    Blocking output (inv [8:0])  As you can see, the blocking output leads to no information being taken in after the first set. I stays the same the whole time.(code for this problem is on page 3).    Non-blocking output (inv [9:0])    Blocking output (inv [9:0])  WHAT HAPPENS TO THE z OUTPUT WITH 10 INVERTERS?  I get the same output when I do 10 bits, doesn’t seem to like it. This is because the number of inverters has to be even.  WHAT IS THE REPORTED DIFFERENCE BETWEEN CURSORS ON TWO CONSECUTIVE RISING EDGES? 3600ps      Finally, this is the code I used for this problem. |

**Section 2 – Hazard Detection**

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| The bottom line is my output. There is one hazard right before 20000ps, and I used brute force.  The hazard is on A when going from 1110 to 0110, but it does not work the other way. |

**Section 3 – Rule for Verilog**

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| Does it hold the Q output low, as required?   * No, as you can see, there are multiple examples where the Q output does not remain low.   Modified JKFF module: As you can see, the output remains low on clear being high. |

**Section 4 – FSM Coding**

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| At 40nsec, Sh goes high when N goes high.    This is the code I generated for #4 |

**Section 5 – Verilog 6:1 MUX**

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| As you can see, there are 6 distinct patters on the output.  Here is the code that I generated for the 6:1 MUX: |

**Section 6 – Delays**

Waveform screenshot at time t = 0 and 100 ns. I will refrain from providing code as it was provided in the assignment document.

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| Figure 6.1: Output at t = 0ns, I = 0, X, Y, Z are unknown.    Figure 6.2: Output at 100ns, I = 0, X, Y, Z = 1. |